Projekt "Perspektywy Współpraca Synergia Zarządzanie w Tarnowie" współfinansowany jest przez Unię Europejską ze środków Europejskiego Funduszu Społecznego w ramach Programu Operacyjnego Wiedza Edukacja Rozwój. Projekt realizowany w ramach konkursu Narodowego Centrum Badań i Rozwoju z III Osi priorytetowej: Szkolnictwo wyższe dla gospodarki i rozwoju; Działanie 3.5 Kompleksowe programy szkół wyższych. Nr umowy o dofinansowanie projektu: POWR.03.05.00-00-Z087/17-00.

Module SYLLABUS

Organizational unit name	The Polytechnic Institute – Department of Electronics and Telecommunications		
Field of study	Electronics and Telecommunications		
Module name	Hardware implementation of algorithms		
Module code	POWER.IP.9	**Erasmus code**	6.5
ECTS	3	**Module type**	Optional
Year of study	4	**Semester**	7

Form of classes	**Hours total**	**Form of assessment**
Project classes	30	Graded credit

Coordinator teacher	PhD Łukasz Mik		
Academic teacher	PhD Łukasz Mik		
Language of instruction	English		
Basic courses	No	**Open course / course at he another field of study**	No
Profile of education	Practical profile	**Study level**	First-cycle level

Prerequisites and additional requirements

Previous courses:
- Electronic devices
- Digital electronics
- Digital signal processing
- Microprocessor technology
- Programming methods and techniques

Additional requirements:
- Basic knowledge of C language
- Ability to use measuring devices such as: oscilloscope, digital multimeter etc.

Learning outcomes for module

No.	**Student after module completion has the knowledge/knows how to/is able to Learning outcome code**	**Learning outcome type**	**Method of learning outcomes verification**	**Form of classes**
				Project
1.	Is able to formulate the specification of simple electronic and telecommunications systems at the level of performed functions, also with the use of hardware description languages	Skills	Project, technical documentation	Y
2.	Is able to formulate an algorithm, uses high and low level programming languages and appropriate IT tools to develop computer programs that control the electronic system and software for microcontrollers or control microprocessors	Skills	Project	Y

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3.	Can acquire information from literature, databases and other sources; can integrate the obtained information, make their interpretation, as well as draw conclusions and formulate and justify opinions	Skills	project	Y
4.	Can work individually and in a team; knows how to estimate the time needed to complete the task ordered; is able to develop and implement a schedule of work to ensure that deadlines are met.	Skills	project	Y
5.	Is able to develop documentation on the implementation of the engineering task and prepare a text containing a discussion of the results of this task; can prepare and present a short presentation devoted to the results of the engineering task	Skills	Technical documentation	Y
6.	Is aware of the responsibility for his own work and readiness to comply with the rules of working in a team and taking responsibility for the tasks he has carried out jointly	Social competence	Project	Y

Didactic methods

Form of classes:
The project is implemented in two-person groups. All groups are obliged to present individual stages of the project during the semester.

Teaching methods:
The project carried out in stages, which are regularly verified by the teacher. Motivating to ask questions and solve them on the class forum - brainstorming.

Rules of assessment

In order to pass the project, the last week of the semester students should present a working device with implemented algorithm on embedded platform with FPGA chip. The grades are issued in accordance with the current regulations of studies at the State Higher Vocational School in Tarnow based on the design and complete technical documentation confirming its implementation.

Module content (brief)

In this module project classes are carried out with the following stages:

1. Choice of topic and specification of requirements for the final result of the project
2. Analysis of requirements and selection of appropriate tools and platform with FPGA chip
3. Describing the principle of operation of the electronic system in the algorithm form.
4. Implementation of algorithm in VHDL language
5. Preparation of test vectors for system simulation. Carrying out the necessary tests.
6. Programming of selected FPGA chip with configuration file. Carrying out the tests with measurement devices.
7. Preparation of project documentation

Module content (comprehensive)

1. Choice of topic and specification of requirements for the final result of the project

The list of problems covers a wide range of knowledge in the field of embedded systems and implementation of algorithms in fast FPGA chips. Students can choose 1 of 10 topics:

- Tachometer with result presentation on the 7-segment LED display
- Programmable PWM generator
- Hardware CRC generator
- Simple camera with VGA output
- Sinusoidal signal generator with direct digital synthesis
- Hardware implementation of the XOR streaming cipher
- WAV audio file player based on the PicoBlaze soft-processor
- Pseudorandom sequence generator for testing communication interfaces
- Converter of serial interface to parallel and vice versa.
- BMP file display on a VGA monitor based on the PicoBlaze soft-processor

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2. Analysis of requirements and selection of appropriate tools and platform with FPGA chip

   The choice of the right platform is closely related to the clock frequency of the FPGA chip, which will ensure fast data processing and signal transmission. Students implement the project on one of three evaluation boards to choose from:
   - Digilent Virtex-II Pro, with Xilinx Virtex II Pro device clocked at 100 MHz.
   - Numato Elbert v2 – with Xilinx Spartan3A device clocked at 12 MHz.
   - Lattice iCEstick – with Lattice iCE40HX device clocked at 12 MHz.

3. Describing the principle of operation of the electronic system in the algorithm form.

   Presentation of the principle of operation of the designed system using the algorithm block diagram.

4. Implementation of algorithm in VHDL language

   Translating the block diagram of the algorithm into VHDL description. Creating an appropriate hierarchy of blocks within a project. Correct propagation of the global clock signal between architecture blocks. Reading asynchronous signals at the system input in accordance with the rules of metastability prevention. Assignment of signals inside the architecture defined as outputs to the corresponding pins of the FPGA. Use of auxiliary function blocks such as digital clock manager, three-state buffers, RAM and ROM block memory.
   In order to implement algorithms in VHDL the ISE WebPack software package is used for Xilinx systems and the iCEcube2 package for Lattice systems.

5. Preparation of test vectors for system simulation. Carrying out the necessary tests.

   Editing test vectors using the Testbench Waveform editor. Functional and time simulation.

6. Programming of selected FPGA chip with configuration file. Carrying out the tests with measurement devices.

   Generating the *.bit configuration file and programming the target system. Analysis of signals using a logic analyzer and oscilloscope.

7. Preparation of project documentation

   The document confirming the implementation of the project should include: analysis of the problem, justification of choosing the FPGA type and software, description of the most important parts of implementation in VHDL language, simulation and measurement results.

Recommended literature and teaching resources

1. Zbysiński P., Majewski J., Układy FPGA w przykładach, Wydawnictwo BTC, Warszawa 2007.
2. Chu P. P., FPGA prototyping by VHDL examples, John Wiley & Sons, 2008
3. Nowakowski M., PicoBlaze. Mikroprocesor w FPGA, Wydawnictwo BTC, 2009
4. Datasheets of Xilinx Virtex-II Pro, Xilinx Spartan3A and Lattice iCE40XH

Connection with area of study	engineering sciences
Student workload (ECTS credits balance)	
Student workload form	Student workload [hours]
Participation in project classes	30
Completion of a project	35
Individual consultations and final project presentation	10
Summary student workload	75
Module ECTS credits	
Workload of the direct assistance of the academic teacher	**1.6**
Workload of the practical classes	**3**

Annotation:
1 hour = 45 minutes